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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,554	04/19/2006	Eduard Ferdinand Stikvoort	NL03 1244 US1	3883

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
09/23/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/576,554	STIKVOORT ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the RCE filed 8/15/2008. Claims 1-4 are under examination.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the recitation of "wherein the second inverted output is coupled to the first set input for providing an inverted output signal from said second non-inverted output of the second flip-flop as feedback to the set input of the first flip-flop" is indefinite because it is unclear as to what the applicant means. Figure 3 shows the second inverted output (Qa2) is coupled to the first set input (gate of the transistor M3) and the transistor M3 provides the first non-inverted output Q1. Thus, it is unclear as to how the inverted output signal is provided from said second non-inverted output of the second flip-flop as recited. Clarification and correction are required.

In claims 3-4, the recitation of "a third output Qa2" is indefinite because it is unclear if the third output is different than the second inverted output recited in claim 1.

Claim 2 is indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's cited prior art figure 2.

Applicant's cited prior art figure 2 shows a frequency divider comprising a first flip flop without stacked transistors (M1-M4) having a first clock input (CL/) for receiving a clock signal, the first flip flop further comprising a first set input (gate of M3) and a first non-inverted output (Q1), a second flip flop without stacked transistors (M1'-M4', M5, M6) having a second clock signal (CL) for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted to the first clock input, a second set input (gate of M3') coupled to the first non-inverted output, a second non-inverted output (Q2), a second inverted output (Q4), wherein the second inverted output is coupled to the first set input for providing an inverted output signal from said second non-inverted output of the second flip-flop as feedback to the set input of the first flip-flop, insofar as being understood as the second inverted output being coupled to the first set input for providing an inverted output signal (Q4) from the second flip flop to the set input of the first flip flop, wherein the frequency divider does not have an additional controlled inverter for providing a time delay as called for in claim 1.

Regarding claim 2, wherein a period of the second clock signal is the same order of magnitude as a delay through the second inverted output (M5, resistor) of the divider.

Regarding claims 3-4, figure 2 shows a controllable switch (M6) coupled to a third output (Q4) to the first set input of the first flip flop (gate of the transistor M3) and a resistive means.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray (EP 270191) in view of Edwards (US 2005 0156643), both prior art of record.

Figure 5 of Murray shows a frequency divider comprising a first flip flop (1) having a first clock input (C) and a first set input (D), a second flip flop (2) having a second clock input (C) for receiving a second clock signal (output of inverter 5), second set input (D), second inverted output (Q/) and second non-inverted output (Q), the second inverted output being fed back to the set input of the first flip flop.

Murray's figure 5 does not show the first and second flip flop circuits without stacked transistors as called for in claim 1.

Figure 1 of Edwards shows a flip flop circuit without stacked transistors having minimal number of transistors consumption a least amount of power. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to implement Murray's first and second flip flop circuits with the flip flop circuits of Edwards for the purpose of minimizing power consumption.

Regarding claim 2, wherein a period of the second clock signal is the same order of magnitude as a delay through the second inverted output of the divider.

Response to Arguments

5. Applicant's arguments filed 8/15/2008 have been fully considered but they are not persuasive. Applicant argues that the present invention different from prior art figure 2 in that the prevent invention eliminates transistor M5 and M6. However, the current limitations recited in the claim do not distinguish over prior art figure 2. Therefore, the rejection of claims 1-4 as being anticipated applicant's cited prior art figure 2 is deemed proper.

Regarding the rejection of claims 1-2 under 35USC 103(a) as being unpatentable over Murray (EP 270191) in view of Edwards (US 2005 0156643), applicant argues that delay circuit 4, Murray's figure 1, provides a delay time is not persuasive. The delay circuit is used to invert the clock signal which is required for the operation of the second flip flop. It does not provides a time delay. Therefore, the rejection is deemed proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

9/16/2008